

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1           **Claim 1 (original):**    A broadband modulation PLL  
2    comprising:

3           a PLL portion containing a voltage controlled  
4    oscillator, a frequency divider for dividing the frequency  
5    of an output signal of the voltage controlled oscillator,  
6    a phase comparator for comparing the output of the  
7    frequency divider with a reference signal, and a loop  
8    filter for averaging the output of the phase comparator;

9           a first modulation input portion for inputting a first  
10   modulation signal to a first position of the PLL portion on  
11   the basis of input modulation data; and

12          a second modulation input portion for inputting a  
13   second modulation signal to a second position different  
14   from the first position of the PLL portion on the basis of  
15   the modulation data, wherein the first modulation signal  
16   input to the first position of the PLL portion is added  
17   with the second modulation signal at the second position,  
18   and any one of the first and second modulation input  
19   portions inverts the phase of the modulation data and  
20   inputs the modulation signal to the PLL portion at the time  
21   of a modulation timing adjustment to adjust the modulation  
22   timing of the first modulation signal and the second

23 modulation signal.

1           **Claim 2 (original):** The broadband modulation PLL  
2 according to claim 1, wherein any one of the first  
3 modulating portion and the second modulating portion has an  
4 inverter for inverting the phase of the modulation data.

1           **Claim 3 (currently amended):** The broadband modulation  
2 PLL according to claim ~~1-or-2~~, wherein at least one of the  
3 first modulating portion and the second modulating portion  
4 has a delay circuit for adjusting the output timing of the  
5 modulation signal.

1           **Claim 4 (currently amended):** The broadband modulation  
2 PLL according to ~~any one of claims 1 to 3~~claim 1, wherein  
3 the first modulation input portion generates a  
4 frequency-dividing ratio of the frequency divider as the  
5 first modulation signal and outputs the first modulation  
6 signal to the frequency divider, and the second modulation  
7 input portion outputs the second modulation signal to the  
8 input side of the voltage controlled oscillator.

1           **Claim 5 (currently amended):** The broadband modulation  
2 PLL according to ~~any one of claims 1 to 4~~claim 1, further  
3 comprising a timing controller for generating a modulation  
4 timing control signal to adjust the modulation timing of

5 the first modulation signal and the second modulation  
6 signal.

1 Claim 6 (original): The broadband modulation PLL  
2 according to claim 5, wherein the timing controller  
3 generates the modulation timing control signal on the basis  
4 of the input signal of the voltage controlled oscillator.

1 Claim 7 (original): The broadband modulation PLL  
2 according to claim 5, wherein the timing controller  
3 generates the modulation timing control signal on the basis  
4 of the output signal of the voltage controlled oscillator.

1 Claim 8 (original): The broadband modulation PLL  
2 according to claim 5, further comprising:

3 a measuring unit for demodulating the output signal of  
4 the PLL portion and calculating an amplitude value;

5 an operator for calculating a timing error on the  
6 basis of the amplitude value calculated by the measuring  
7 unit; and

8 a storage unit for storing a timing set value for  
9 controlling the timing of at least one of the first  
10 modulation input portion and the second modulation input  
11 portion which is calculated on the basis of the timing  
12 error, wherein the first modulation input portion and the  
13 second modulation input portion control the modulation

14        timing on the basis of the set value set in the storage  
15        portion.

1            **Claim 9 (currently amended):**    A modulation system  
2        having the broadband modulation PLL according to ~~any one of~~  
3        ~~claims 1 to 8~~claim 1.

1            **Claim 10 (currently amended):**    A radio communication  
2        device having the broadband modulation PLL according to ~~any~~  
3        ~~one of claims 1 to 8~~claim 1.

1            **Claim 11 (currently amended):**    A timing correcting  
2        system for a broadband modulation PLL, comprising:  
3            the broadband modulation PLL according to ~~any one of~~  
4        ~~claims 1 to 4~~claim 1; and  
5            a measuring portion for demodulating an output signal  
6        of the broadband modulation PLL and calculating an  
7        amplitude value, wherein the broadband modulation PLL has  
8        an operating portion for calculating the timing error  
9        between the first modulation signal and the second  
10       modulation signal on the basis of the amplitude value  
11       calculated by the measuring portion, and a storage portion  
12       for storing a timing set value for controlling the  
13       modulation timing of at least one of the first modulation  
14       input portion and the second modulation input portion which  
15       is calculated on the basis of the timing error.

1           **Claim 12 (original):** A timing correcting system for  
2       a broadband modulation PLL, comprising:  
3           a broadband modulation PLL;  
4           a measuring portion for demodulating an output signal  
5       of the broadband modulation PLL and detecting a value  
6       indicating modulation precision; and  
7           a measuring unit for demodulating an output signal of  
8       the PLL portion and calculating an amplitude value, wherein  
9       the broadband modulation PLL comprises a PLL portion  
10      containing a voltage controlled oscillator, a frequency  
11      divider for dividing the frequency of an output signal of  
12      the voltage controlled oscillator, a phase comparator for  
13      comparing the output of the frequency-divider with a  
14      reference signal, and a loop filter for averaging the  
15      output of the phase comparator, a first modulation input  
16      portion for inputting a first modulation signal to a first  
17      position of the PLL portion, a second modulation input  
18      portion for inputting a second modulation signal to a  
19      second position different from the first position of the  
20      PLL portion on the basis of the modulation data, an  
21      operating portion for calculating a timing error on the  
22      basis of the amplitude value measured by the measuring  
23      unit, and a storage portion for storing a timing set value  
24      for controlling the output time of at least one of the  
25      first modulation input portion and the second modulation

26 input portion which is calculated on the basis of the  
27 timing error, thereby adjusting a modulation timing, the  
28 first modulation input portion and the second modulation  
29 input portion being controlled so that the timing error is  
30 corrected on the basis of the timing set value set in the  
31 storage portion.

1           **Claim 13 (original):** A timing error correcting method  
2 in broadband modulation PLL comprising:  
3           a step of inputting to different two points in PLL  
4 modulation data which are opposite to each other in phase;  
5           a step of adding modulation signals based on the  
6 modulation data;  
7           a step of detecting the timing error between the  
8 respective modulation signals on the basis of the added  
9 modulation signals; and  
10           a step of correcting an output timing of at least one  
11 of the two-point modulations input to the PLL on the basis  
12 of the detected timing error.

1           **Claim 14 (original):** An adjusting method of a radio  
2 communication device having a broadband modulation PLL for  
3 applying modulation to different two points of PLL,  
4 comprising:  
5           a step of setting a modulation timing of the broadband  
6 modulation PLL, wherein the modulation timing setting step

7 comprises a step of inputting to different two points of  
8 PLL modulation data which are opposite in phase to each  
9 other, a step of outputting a modulation signal of the  
10 broadband modulation PLL on the basis of the modulation  
11 data, a step of demodulating the modulation signal of the  
12 broadband modulation PLL to achieve an amplitude value, a  
13 step of detecting the timing error between the respective  
14 modulation signals and setting a timing set value into a  
15 storage portion provided to the broadband modulation PLL,  
16 and a step of correcting a timing of at least one of the  
17 two-point modulations input to the PLL.

1 **Claim 15 (original):** An adjusting method of a radio  
2 communication device having a broadband modulation PLL for  
3 applying modulation to different two points of PLL,  
4 comprising:

5 a step of setting a modulation timing of the broadband  
6 modulation PLL, wherein the modulation timing setting step  
7 comprises a step of inputting modulation data to different  
8 two points of PLL, a step of outputting modulation signals  
9 of the broadband modulation PLL on the basis of the  
10 modulation data, a step of demodulating a modulation signal  
11 of the broadband modulation PLL and detecting a value  
12 indicating a modulation degree, a step of detecting the  
13 timing error between the respective modulation signals on  
14 the basis of a value indicating the modulation precision

15        and setting a timing set value into a storage portion  
16        provided to the broadband modulation PLL, and a step of  
17        correcting a timing of at least one of the two-point  
18        modulations input to the PLL.